Shri Vaishnav Vidyapeeth Vishwavidyalaya
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) Scheme in the light of NEP-2020
M.Tech. (VLSI Design)

SEMESTER-II (2025-2027)

S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
							THEORY			PRACTICAL		
			L	T	P		End Sem Unversity Exam (60%)	Two Term Exam (20%)	Teachers Assess-ment* (20%)	End Sem Unversity Exam (60%)	Teachers Assess-ment* (40%)	
1	MTVD201	VLSI Testing and Testability	2	1	2	4	60	20	20	30	20	150
2	MTVD202	VLSI Design Flow: RTL to GDS	3	0	2	4	60	20	20	30	20	150
3	MTVD203	Analog VLSI Design	3	0	0	3	60	20	20	30	20	150
4	MTRM301	Research Methodology in Engineering	3	1	0	4	60	20	20	0	0	100
5	-	Elective II	3	0	0	3	60	20	20	0	0	100
6	-	Generic Elective	3	0	0	3	60	20	20	0	0	100
8	MTVD205	Comprehensive Viva	0	0	2	1	0	0	0	30	20	50
TOTAL			**17**	**2**	**4**	**21**	**360**	**120**	**120**	**90**	**60**	**750**

Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical

***Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

Elective II

S. No.	Course Code	Course Name
1	MTVD214	Advanced DSP for VLSI
2	MTVD224	Embedded Computing Principal
3	MTVD234	Product Design Thinking Framework

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Shri Vaishnav Vidyapeeth
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